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## What is claimed is:

1	1. A stacked gate flash memory cell, comprising:
2	a substrate having a trench therein;
<b>3</b>	a conductive layer disposed on the bottom of the
4	trench;
5	a pair of source regions, each disposed in the
6	substrate adjacent to one sidewall of the
7	trench and electrically connected by the
8	conductive layer;
9	a source isolation layer disposed on the conductive
o	layer;
1	a pair of tunnel oxide layers, respectively disposed
2	on one sidewall of the trench and the source
3	isolation layer;
4	a U-shaped floating gate disposed on the source
5	isolation layer, contacting the tunnel oxide
6	layers thereby;
7	a pair of control gate spacers, respectively
8	disposed on each vertical portion of the U-
9	shaped floating gate, substantially having the
0	same width as the vertical portions;
1	a U-shaped inter-gate dielectric layer disposed or
2	the U-shaped floating gate and the control gate
3	spacers;
4	a control gate disposed in the U-shaped inter-gate
5	dielectric; and
6	a drain region disposed in the substrate adjacent to
7 .	the trench.

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- 2. The cell as claimed in claim 1, wherein the substrate is P-type silicon substrate.
- 3. The cell as claimed in claim 1, wherein a bottom insulating layer is further disposed under the conductive layer.
- 1 4. The cell as claimed in claim 3, wherein the bottom insulating layer is silicon dioxide.
  - 5. The cell as claimed in claim 1, wherein the conductive layer is N-type dopant doped polysilicon.
    - 6. The cell as claimed in claim 1, wherein the source isolation layer is silicon dioxide.
    - 7. The cell as claimed in claim 1, wherein the tunnel oxide layer is silicon dioxide.
      - 8. The cell as claimed in claim 1, wherein the U-shaped floating gate and the control gate are N-type dopant doped polysilicon.
- 9. The cell as claimed in claim 1, wherein the U-shaped inter-gate dielectric layer is silicon dioxide.
  - 10. The cell as claimed in claim 1, wherein the control gate spacer is silicon.
- 1 11. A method of fabricating stacked gate flash
  2 memory cells, comprising the steps of:
- providing a substrate;
- forming a plurality of parallel long trenches along a first direction in the substrate;

6	forming a conductive layer and a pair of source
7	regions on the bottom of each long trench,
8	wherein the source regions are respectively
9	disposed in the substrate adjacent to two
10	sidewalls of each long trench and electrically
11	connected by the conductive layer therein;
12	forming a source isolation layer on each conductive
13	layer;
14	forming a tunnel oxide on two sidewalls of each long
15	trench;
16	forming a U-shaped floating gate on each source
17	isolation layer, contacting the tunneling oxide
18	layers;
19	forming a pair of control gate spacers respectively
20	disposed on the vertical portion of the U-
21	shaped floating gate, substantially having the
22	same width as the vertical portions;
23	forming an U-shaped inter-gate dielectric layer on
24	each U-shaped floating gate and the control
25	gate spacers;
26	forming a control gate in each U-shaped inter-gate
27	dielectric layer;
28	forming a plurality of parallel shallow trench
29	isolation (STI) regions along a second
30	direction, defining a plurality of cell
31	trenches; and
32	forming a drain region in the substrate adjacent to
33	each cell trench.

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- 1 12. The method as claimed in claim 11, wherein the first direction is perpendicular to the second direction.
  - 13. The method as claimed in claim 11, wherein the substrate is P-type silicon substrate.
    - 14. The method as claimed in claim 11, further comprising before forming a plurality of parallel long trenches along a first direction in the substrate, the step of sequentially forming a pad oxide layer and a mask layer on the substrate.
    - 15. The method as claimed in claim 14, wherein the mask layer is silicon nitride.
      - 16. The method as claimed in claim 14, wherein the pad oxide layer is silicon dioxide.
      - 17. The method as claimed in claim 11, further comprising before forming a conductive layer and a pair of source regions on the bottom of each long trench, the step of forming a bottom insulating layer on the bottom of each long trench.
      - 18. The method as claimed in claim 11, wherein forming a conductive layer and a pair of source regions on the bottom of each long trench further comprises the steps of:

forming a source material layer in each long trench; performing a thermal annealing process on the source material layer, driving out dopants therefrom, forming a pair of source regions in the

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9	substrate adjacent to two sidewalls of each
10	long trench, electrically connected by the
11	conductive layer therebetween; and
12	removing the source material layer from each long
13	trench.
1	19. The method as claimed in claim 18, wherein the
2	source material layer is N-type doped polysilicon.
1	20. The method as claimed in claim 19, wherein the
2	N-type doped polysilicon comprises phosphorous (P) doped
3	polysilicon or arsenic (As) doped polysilicon.
1	21. The method as claimed in claim 11, further
. 2	comprising before forming a tunnel oxide on two sidewalls
3	of each long trench, the step of performing a threshold
4	voltage implantation on the sidewalls of each long
5	trench.
1	22. The method as claimed in claim 11, wherein
2	forming a U-shaped floating gate on the source isolation
3	layer, contacting the tunnel oxide layers further
4	comprises the steps of:
5.	conformably depositing a floating gate layer in each
6	long trench;
7	forming a protective layer on the floating gate
8	layer in each long trench, exposing portions of
9	the floating gate layer; and
10	removing portions of the floating gate layer exposed
11	by the protective layer, forming a U-shaped
12	floating gate therein.

- 23. The method as claimed in claim 22, wherein the protective layer is boro-silicate-glass (BSG).
  - 24. The method as claimed in claim 11, wherein forming a pair of control gate spacers, each disposed on the vertical portion of the U-shaped floating gate, having the same width as the vertical portions further comprises the steps of:
    - conformably depositing materials of a control gate spacer layer;
    - etching the materials of the control gate spacer layer, stopping at the protective layer in each long trench, forming a control gate spacer disposed on each vertical portion of each U-shaped floating gate, substantially having a same width as that thereof; and removing the protective layer therein.
  - 25. The method as claimed in claim 24, wherein the method for removing the protective layer is wet etching.
  - 26. The method as claimed in claim 25, wherein the control gate spacer is silicon dioxide.
  - 27. The method as claimed in claim 11, wherein forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches, further comprises the steps of:
- sequentially performing photolithography and etching, defining a plurality of parallel long

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8	isolation trenches along a second direction,
9	stopping at the source isolation layer therein;
10	and
11	forming an insulating layer in each long isolation
	trench.
1	28. The method as claimed in claim 27, wherein the
2	insulating layer is silicon dioxide.
1	29. The method as claimed in claim 27, wherein the
2	method of forming the insulating layer is high density
3	plasma enhanced chemically vaporization deposition (HDP
4	CVD).
1	30. The method as claimed in claim 12, wherein
2	forming a drain region in the substrate adjacent to each
3	of the cell trenches further comprises the steps of:
4	removing the mask layer, exposing the pad oxide
.5	layer;
.6	performing a drain implantation;
7	performing a thermal annealing process, forming a
8	drain region in the substrate adjacent each
9	cell trenches;
10	removing the pad oxide layer; and
11	forming a second insulating layer on each drain
12	region.
1	31. The method as claimed in claim 30, wherein
2	impurities used in the drain region implantation are N-
3	type impurities.

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32.	The m	method as	claimed	in claim	31, w	vherein	the
N-type	impurit	cies com	prise pl	nosphorous	(P)	ions	or
arsenic	(As) io	ns.					

33. The method as claimed in claim 30, wherein the method for forming the second insulating layer is low pressure chemical vapor deposition (LPCVD).